IN THE CLAIMS

Please amend the Claims as follows:

1. (TWICE AMENDED) A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

providing a contact region in or on a substrate;

depositing a liner layer overlying said contact region;

depositing a dielectric layer overlying said liner layer wherein all portions of said dielectric layer have a dielectric constant less than 2.5;

first etching said damascene opening through said dielectric layer to said liner layer overlying said contact region wherein said first etching comprises a high F/C ratio etch chemistry, high power, and low pressure; and

second etching said liner layer within said damascene opening to expose said contact region wherein said second etching comprises a high F/C ratio etch chemistry, low power, and low pressure to complete formation of said damascene opening in said fabrication of said integrated circuit device.

15. (TWICE AMENDED) A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

providing a contact region in or on a substrate;

depositing a liner layer overlying said contact region;

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5 and wherein no etch stop layer is used within said dielectric layer;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry, power of 15 between 700 and 1000 watts, and pressure of between 20 and 150 mTorr and wherein a high polymer gas is not used; and

second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr to complete formation of said damascene opening in said fabrication of said integrated circuit device.

24. (TWICE AMENDED) A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing a contact region in or on a substrate;

depositing a liner layer overlying said contact region;

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry of CF_4, O_2, and Ar gases, power of between 700 and 1000 watts, and pressure of between 20 and 150 mTorr and wherein a high polymer gas comprising C_4F_8, CH_2F_2, C_2F_2, or C_2F_6 is not used;

second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr;

depositing a barrier metal layer within said damascene opening;

depositing a copper layer overlying said barrier metal layer; and

polishing down said copper layer and said barrier metal layer to leave said barrier metal layer and said copper layer only within said damascene opening to complete said copper metallization in said fabrication of said integrated circuit device.